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Thermal Modeling using SPICE

April 2015

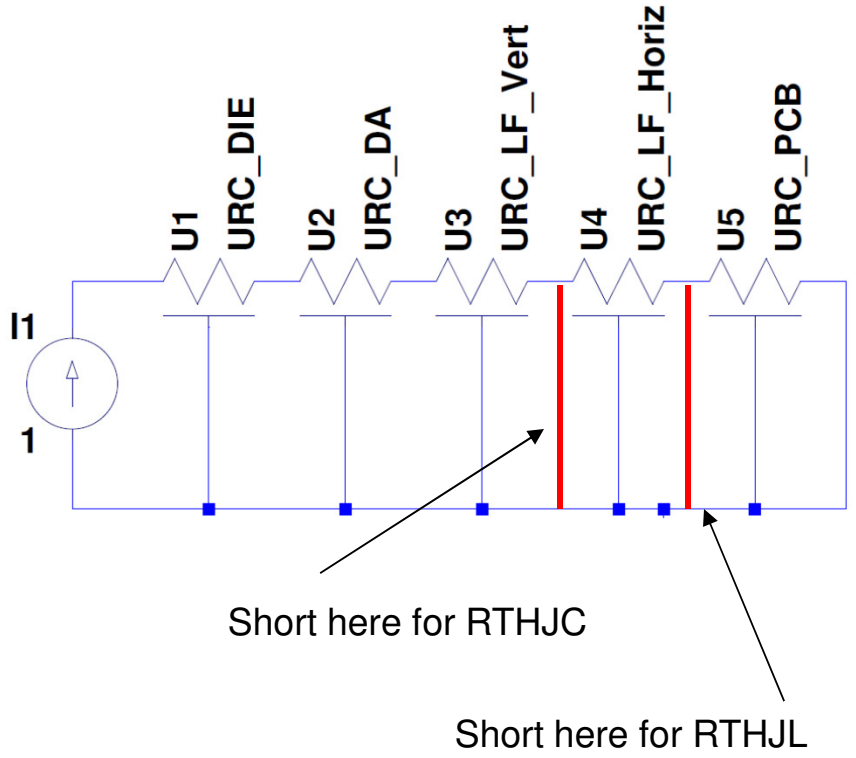
Concept

- Use up to 5 Uniform Resistor Capacitor (URC) elements to model RTH:
  1. Die (vertical heat flow)
  2. Die attach
  3. Lead Frame vertical heat flow (copper under die)
  4. Lead Frame horizontal heat flow (not included in RTHJC for DFN DPak, included in RTH JL for SO-8, includes some lateral flow for DFN & DPAK on PC Board as leadframe works as a heat spreader)
  5. PC Board (somewhat fixed but small footprint devices have a higher resistance due to small periphery near foot)

Advantages of Model

By using URC elements with defined applicability, this method allows:

- Re-use of some elements, eg leads, PC board
- Use of the same model for RTH JC and RTHJA
- PC Board thermal models can be added
- URC Model is more accurate than 4 element lumped value models



Netlist (export from LT Spice)

```
1 0 N001 1
U1 N001 N002 0 URC_DIE L=1 N=50
U2 N002 N003 0 URC_DA L=1 N=10
U3 N003 N004 0 URC_LF_Vert L=1 N=10
U4 N004 N005 0 URC_LF_Horiz L=1 N=5
U5 N005 0 0 URC_PCB L=1 N=5
```

- Model values stored in ascii file of model for easy editing
- Force 1A DC and voltage is temp rise for 1W heat = thermal impedance °C/W
- N can be decreased to improve speed, reduce accuracy

Accuracy based on 2.2mm^2 AM4874N R5

Time	RTH SPICE °C/W	RTH DS LIMIT (RTHJA ∞ = 80°C/W+	RTH Old Model °C/W	Notes
1ms	1.15	1.2	1.17	
10ms	3.2	3.6	3.12	
100ms	6.4	10.4	8	Low, C_LF_H high?
1s	16.2	25.6	17.8	
10s	25.8	40	24	
100s	37.5	64	41.5	
500s	48	80	49	

Values Used for Prior Page

Die size mm2	RDIE	CDIE m	RDA	CDA m	R_LF_Vert	C_LF_Vert	R_LF_Horiz	C_LF_Horiz	RPCB	CPCB
2.2	2.27	2.2	0.681818	0.22	1.818	0.02	16	0.08	28	10

Maxes and Aggressiveness

- Based on typical SO-8 RTHJA on 2 x 25mm = 46.2°C/W, so model of 49 °C/W is about right for a small die
- However data sheet gives max of 80 °C/W as it is typ for short pulses and then max for long pulses
- Suggest use model + 15% as limit
- 56 x 1.15 = 65 °C/W a reasonable limit

Package	Observed RTHJA	
	10 mm x 15 mm board	25 mm x 25 mm board
DFN2x3	51.3° C/W	47.7° C/W
DFN3x3	46.2° C/W	39.5° C/W
DFN5x6	38.8° C/W	32.8° C/W
SO-8	52.4° C/W	46.2° C/W
DPAK	-	28.6° C/W

DC RTH JA, JL Sanity Checks

DFN56

Die size mm2	RDIE	CDIE m	RDA	CDA m	R_LF_V	C_LF_V	R_LF_H	C_LF_H	RPCB	CPCB		RTOT JA	RTOT JC
2.2	2.27	2.2	0.681	0.22	1.8181	0.02	5	0.2	26	10		35.7	4.77
10	0.5	10	0.15	1	0.4	0.02	5	0.2	26	10		32.05	1.05

SO-8

Die size mm2	RDIE	CDIE m	RDA	CDA m	R_LF_V	C_LF_V	R_LF_H	C_LF_H	RPCB	CPCB		RTOT JA	RTOT JL
1	5	1	1.5	0.1	4	0.02	16	0.08	28	10		54.5	26.5
2.2	2.272	2.2	0.681	0.22	1.8181	0.02	16	0.08	28	10		48.77	20.77
8	0.625	8	0.187	0.8	0.5	0.02	16	0.08	28	10		45.31	17.31

Assume FDMS85200 is approx 10 $mm^{2,}$ and add ~20% for limit fits with Fairchild spec (and SiRa00) for RTH JC. Experimental Data has shown that RTHJA for medium die DFN 56 is ~ 33°C/W

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Conclusion

- This new model allows calculation of RTHJC, JL and JA and transient curves, even JL curves. And allows non linear input
- By separating die from package performance and allowing plotting of each element, thermal performance can be better understood
- Same model used for RTH JL and JA
- By separating each element, one element may be changed to determine effect, eg model improved performance PC Board
- Thermal Spice models available from Analog Power on a experimental individual basis to ensure accuracy and improvement over time
- Spice can be run at different time steps depending on the granularity needed. Ideally run at step size of 1/10000 of the limit being determined (ie 100n for 1ms)