P-Channel 40-V (D-S) MOSFET

Key Features:

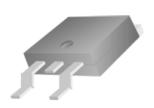
- Low r_{DS(on)} trench technology
- · Low thermal impedance
- · Fast switching speed

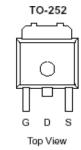
Typical Applications:

- AEC-Q101 qualified and PPAP capable
- Load Switches
- DC/DC Conversion
- Motor Drives

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I _D (A)		
-40	12 @ V _{GS} = -10V	-53		
	16 @ V _{GS} = -4.5V	-46		







ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter			Limit	Units		
Drain-Source Voltage		V_{DS}	-40	W		
Gate-Source Voltage			±20	V		
Continuous Drain Current a	T _C =25°C	I _D	-53	۸		
Pulsed Drain Current ^b		I _{DM}	-200	Α		
Continuous Source Current (Diode Conduction) a			-53	Α		
Power Dissipation ^a	T _C =25°C	P_D	50	W		
Operating Junction and Storage Temperature Range		T_J , T_{stg}	-55 to 175	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	40	°C/W			
Maximum Junction-to-Case	$R_{\theta JC}$	3	C/VV			

1

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

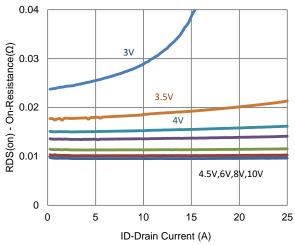
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \text{ uA}$	-1			V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	1	$V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10		
On-State Drain Current a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-80			Α	
Dunin Course On Bosistana a		$V_{GS} = -10 \text{ V}, I_D = -20 \text{ A}$			12	m0	
Drain-Source On-Resistance ^a	r _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -16 \text{ A}$	V _{GS} = -4.5 V, I _D = -16 A		16	mΩ	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -20 \text{ A}$		44		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = -26 \text{ A}, V_{GS} = 0 \text{ V}$		-0.91		V	
		Dynamic ^b					
Total Gate Charge	Q_g	$V_{DS} = -20 \text{ V}, V_{GS} = -4.5 \text{ V},$		49		nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -4.3 \text{ V},$ $I_{D} = -20 \text{ A}$		18			
Gate-Drain Charge	Q_gd	10 - 20 //		14		1	
Turn-On Delay Time	t _{d(on)}	V 20 V D = 1.0		9			
Rise Time	t _r	$V_{DS} = -20 \text{ V}, R_{L} = 1 \Omega,$ $I_{D} = -20 \text{ A},$		11		no	
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = -10 \text{ V}, R_{GEN} = 6 \Omega$		128		ns	
Fall Time	t _f	VGEN = 10 V, IVGEN = 0 12		42			
Input Capacitance	C _{iss}			3810			
Output Capacitance	C _{oss}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		297		pF	
Reverse Transfer Capacitance	C_{rss}			273			

Notes

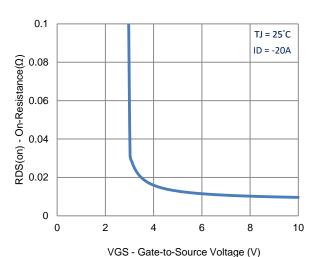
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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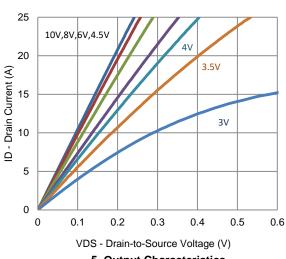
Typical Electrical Characteristics



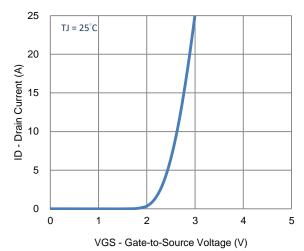
1. On-Resistance vs. Drain Current



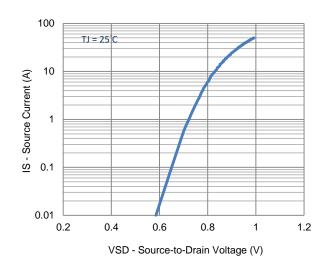
3. On-Resistance vs. Gate-to-Source Voltage



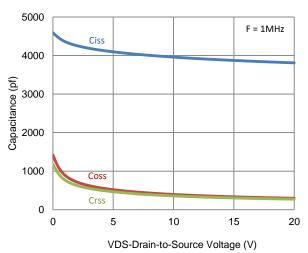
5. Output Characteristics



2. Transfer Characteristics

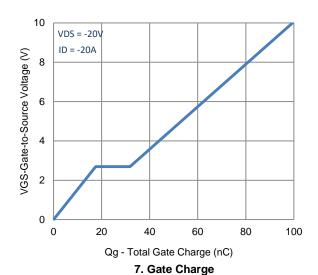


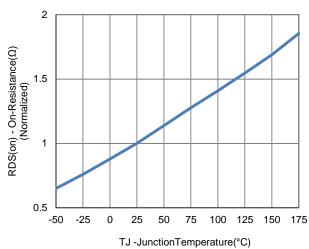
4. Drain-to-Source Forward Voltage

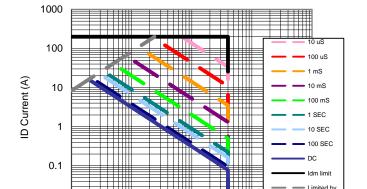


6. Capacitance

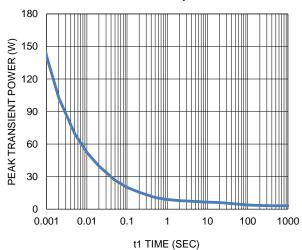
Typical Electrical Characteristics







8. Normalized On-Resistance Vs Junction Temperature



VDS Drain to Source Voltage (V)

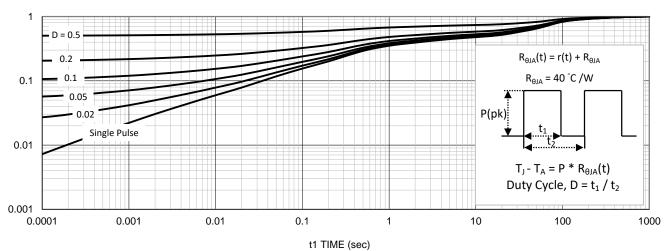
9. Safe Operating Area

10

100

1000

10. Single Pulse Maximum Power Dissipation

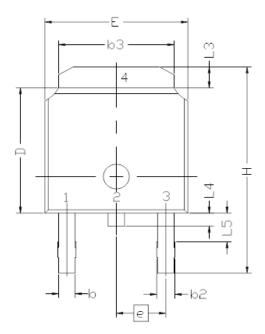


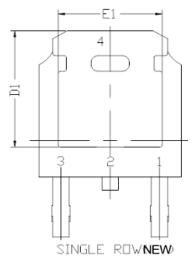
11. Normalized Thermal Transient Junction to Ambient

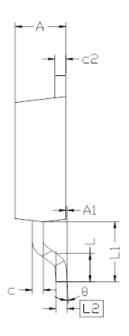
0.01

0.1

Package Information







CVMDEL	DIMENS:	[DNAL	REQMTS
SYMBOL	MIN	NDM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1		.743 R	
_L2		.508 BS	
L3	0,89		1.27
L4	0.64		1.01
L5			
D	6.00	6.10	6.223
Н	9.40	10.00	10.40
b	0.64	0.76	0,88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
е		286 BS	
Α	2,20	2.30	2.38
A1	0		0.127
	0.45	0.50	0.60
c2	0.45	0,50	0.58
D1	5.30		
E1	4.40		
θ	0°		10°

Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.