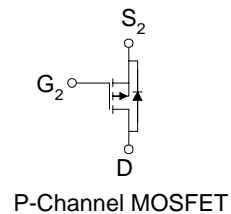
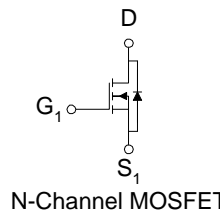
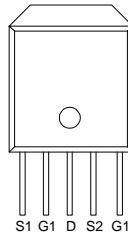


**P & N-Channel 30-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
30	95 @ $V_{GS} = 2.5V$	20
	59 @ $V_{GS} = 4.5V$	24
-26.5	178 @ $V_{GS} = -2.5V$	-14
	118 @ $V_{GS} = -4.5V$	-17

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	$V_{DS}$	30	-26.5	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	
Continuous Drain Current <sup>a</sup>	$T_A=25^\circ C$ $I_D$	24	-17	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	40	-40	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	30	-30	A
Power Dissipation <sup>a</sup>	$T_A=25^\circ C$ $P_D$	50	50	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175		$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
<b>Static</b>							
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 uA	N	0.6			V
		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 uA	P	-0.6			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = -12 V, V <sub>DS</sub> = 0 V	P			±100	nA
		V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V	N			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V	P			-1	uA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	N			1	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	N	20			A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -4.5 V	P	-20			
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A	N			59	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.2 A				95	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.6 A	P			112	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.9 A				172	
Forward Transconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5.0 A	N		25		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -3.6 A	P		10		
<b>Dynamic</b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =5.0A P-Channel V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3.6A	N		6.3		nC
			P		10		
Gate-Source Charge	Q <sub>gs</sub>		N		0.9		
			P		2.2		
Gate-Drain Charge	Q <sub>gd</sub>		N		1.9		
			P		1.7		
<b>Switching</b>							
Turn-On Delay Time	t <sub>d(on)</sub>	N-Chaneel V <sub>DD</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A , R <sub>GEN</sub> =6Ω, P-Channel V <sub>DD</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A R <sub>GEN</sub> =6Ω	N		7.4		nS
			P		7.6		
Rise Time	t <sub>r</sub>		N		4		
			P		6.8		
Turn-Off Delay Time	t <sub>d(off)</sub>		N		22.2		
			P		33.6		
Fall-Time	t <sub>f</sub>		N		3.6		
			P		23.2		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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