D2

P-Channel MOSFET

Analog Power

P & N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN5x6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)} m(\Omega)$	I _D (A)	
40	$46 @ V_{GS} = 4.5V$	7.2	
40	$36 @ V_{GS} = 10V$	8.1	
40	55 @ $V_{GS} = -4.5V$	-6.6	
-40	39 @ $V_{GS} = -10V$	-7.8	
-40			

D1

S

N-Channel MOSFET

SOIC-8PP Top View

8 🖽 D1

7 🗖 D1

6 🖽 D2

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S1 [] 1

G1 🗖 2

S2 🗖 3

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G2



FREE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	N-Channel	P-Channel	Units		
Drain-Source Voltage		V _{DS}	40	-40	v		
Gate-Source Voltage		V _{GS}	20	-20			
Continuous Drain Current ^a	$T_A=25^{\circ}C$	·I _D	8.1	-7.8	А		
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$		6.6	-6.4			
Pulsed Drain Current ^b		I _{DM}	±20	±20			
Continuous Source Current (Diode Conduction) ^a		Is	2.9	-2.9	А		
	$T_A=25^{\circ}C$	D_	3.5	3.5	w		
Power Dissipation ^a	$T_A=70^{\circ}C$	гD	2.2	2.2			
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	35	°C/W		
	Steady State		85	°C/W		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS ($T_A = 2$			\mathbf{Limits}					
Parame te r	Symbol	Test Conditions	Ch Min				Unit	
Static								
Gate-Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}$, $I_D = 250 \text{ uA}$	N	1			v	
	GS(th)	$V_{GS} = V_{DS}, I_{D} = -250 \text{ uA}$	Р	-1			,	
Gate-Body Leakage	I _{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$	Р			±100	nA	
Care Doug Dourage	-035	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	N			±100	117 1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -32 V, V_{GS} = 0 V$	P N			-1	uA	
		$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$	N	20		1		
On-State Drain Current ^A	I _{D(on)}	$\frac{V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}}{V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}}$	P	-20			A	
		$V_{\rm DS} = -3$ V, $V_{\rm GS} = -10$ V V _{GS} = 10 V, I _D = 1 A		-20		36		
Drain-Source On-Resistance ^A		$V_{GS} = 4.5 \text{ V}, \text{ ID} = 1 \text{ A}$	N			46	mΩ	
	r _{DS(on)}	$V_{GS} = -10 \text{ V}, \text{ ID} = -1 \text{ A}$	Р			39	11162	
		$V_{GS} = -4.5 \text{ V}, \text{ ID} = -1 \text{ A}$ $V_{DS} = 15 \text{ V}, \text{ ID} = 1 \text{ A}$	N		40	59		
Forward Tranconductance ^A	g _{fs}	$V_{DS} = -15 \text{ V}, I_D = 1 \text{ A}$ $V_{DS} = -15 \text{ V}, I_D = -1 \text{ A}$	P N		31		S	
Dynamic	1			11				
Total Gate Charge	Qg		N		10			
Total Gate Charge	Qg	N-Channel	P		10		nC	
Gate-Source Charge	Qgs	V_{DS} =15V, V_{GS} =4.5V, I_{D} =1A	N P		3 4			
		P-Channel	N		3			
Gate-Drain Charge	Q_{gd}	VDS=-15V, VGS=-4.5V, ID=-1A	Р		5			
			Ν		3			
Turn-On Delay Time	td(on)	N-Chaneel	Р		3			
Rise Time	tr	$V_{DD} = 15V, V_{GS} = 10V, I_{D} = 1A$,	N		3		1	
		R _{GEN} =25Ω, P-Channel	P N	$ \rightarrow $	3 30		nS	
Turn-Off Delay Time	td(off)	VDD=-15V, VGS=-10V, ID=-1A	P	┟──┤	40			
		$R_{\text{GEN}}=15 \text{ v}, \text{ vGs}=10 \text{ v}, \text{ ID}=1 \text{ A}$	N	1 1	10		1	
Fall-Time	tf		Р		10		1	

Notes

a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

b. Guaranteed by design, not subject to production testing.

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