

P-Channel 20-V (D-S) MOSFET

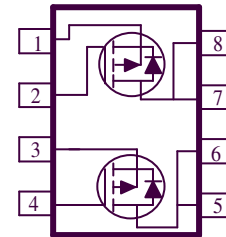
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-20	52 @ $V_{GS} = -4.5V$	-4.9
	89 @ $V_{GS} = -2.5V$	-4.0
	124 @ $V_{GS} = -1.8V$	-3.6

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-5.2	A
	$T_A = 70^\circ\text{C}$		-4.1	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.1	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.1	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case ^a	$t \leq 5 \text{ sec}$	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^a	$t \leq 5 \text{ sec}$	$R_{\theta JA}$	60	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.7			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -4.5 V, V _{GS} = -10 V	-20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -4.9 A			52	mΩ
		V _{GS} = -2.5 V, I _D = -4.0 A			89	
		V _{GS} = -1.8 V, I _D = -3.6 A			124	
Forward Tranconductance ^A	g _{fs}	V _{DS} = -15 V, I _D = -4.9 A		20		S
Diode Forward Voltage	V _{SD}	I _S = 2.5 A, V _{GS} = 0 V		-0.6		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -4.9 A		16.7		nC
Gate-Source Charge	Q _{gs}			1.8		
Gate-Drain Charge	Q _{gd}			1.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 6 Ω , I _D = -1 A, V _{GEN} = -4.5 V		7		nS
Rise Time	t _r			13		
Turn-Off Delay Time	t _{d(off)}			14		
Fall-Time	t _f			9		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

Typical Electrical Characteristics (P-Channel)

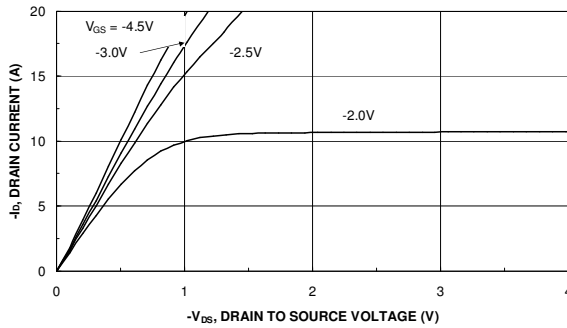


Figure 1. Output Characteristics

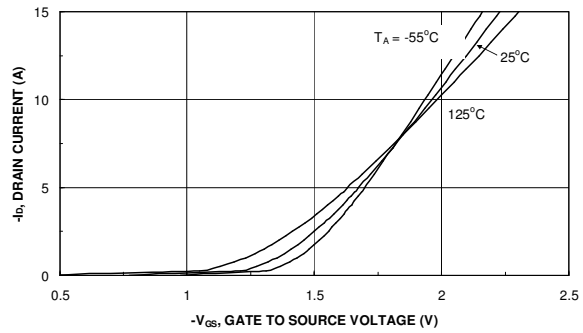


Figure 2. Transfer Characteristics

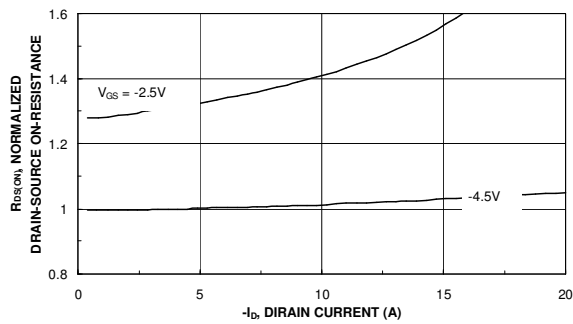


Figure 3. On-Resistance vs. Drain Current

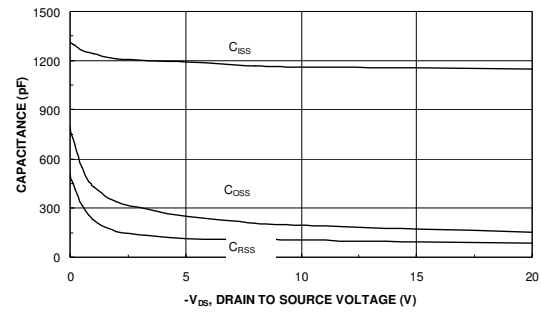


Figure 4. Capacitance

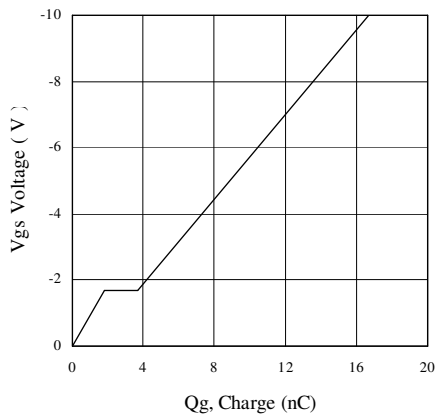


Figure 5. Gate Charge

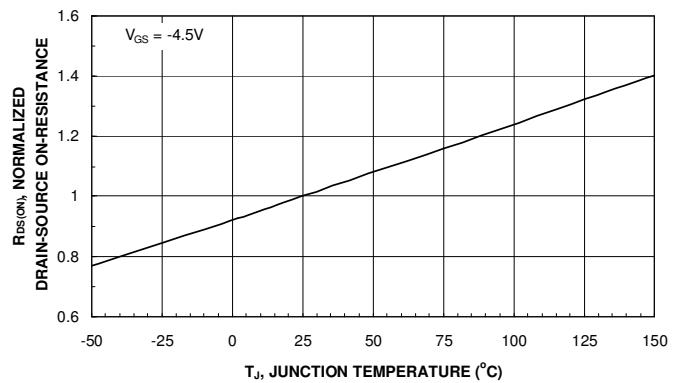


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics (P-Channel)

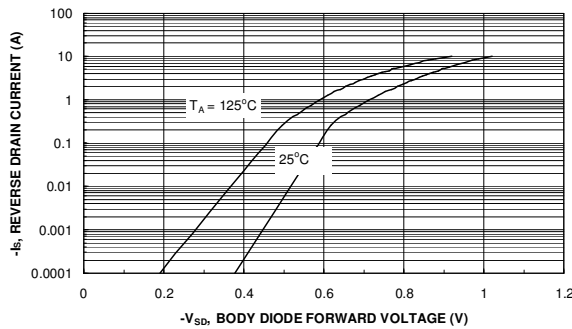


Figure 7. Source-Drain Diode Forward Voltage

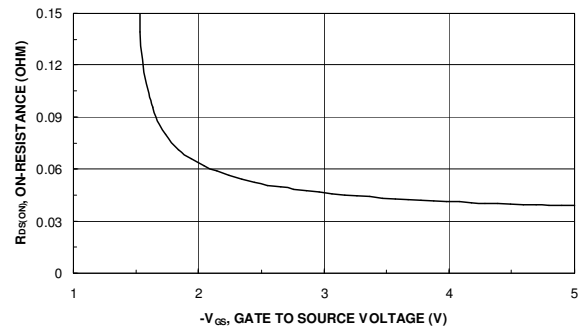


Figure 8. On-Resistance with Gate to Source Voltage

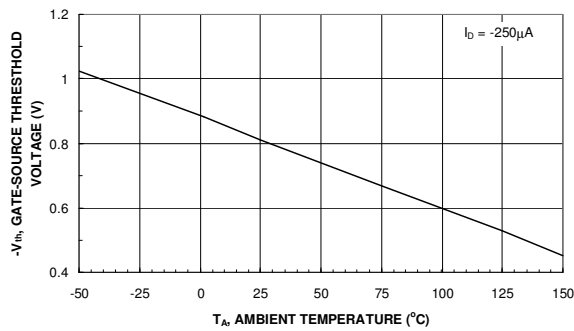


Figure 9. Vth Gate to Source Voltage Vs Temperature

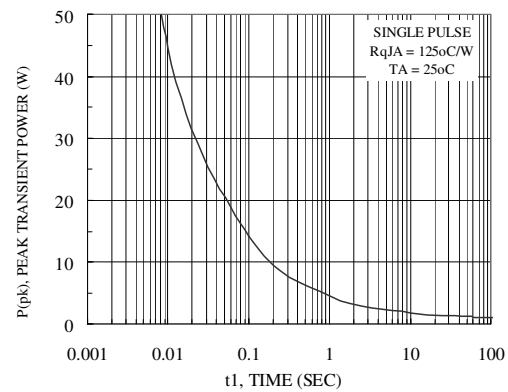


Figure 10. Single Pulse Maximum Power Dissipation

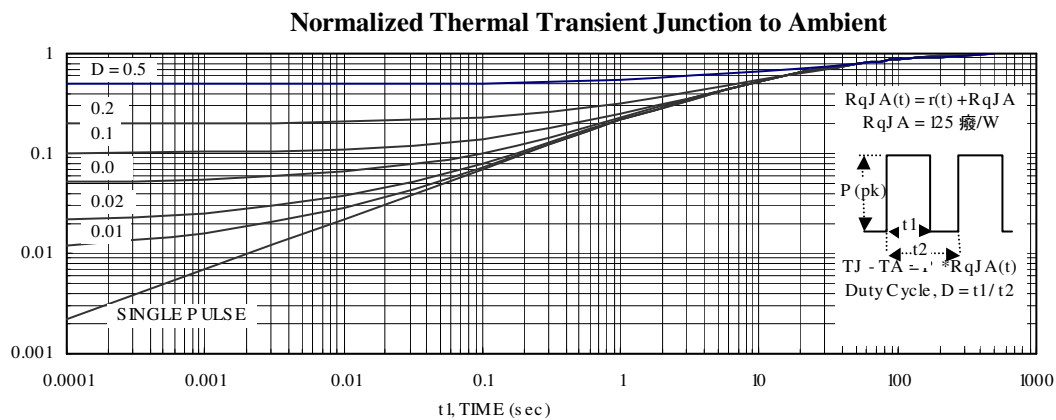
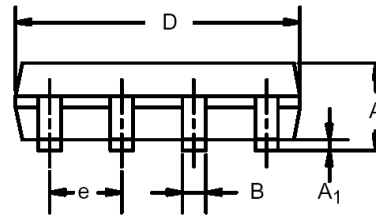
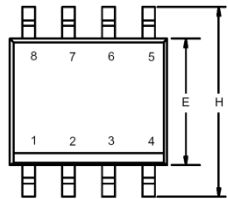


Figure 11. Transient Thermal Response Curve

Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

