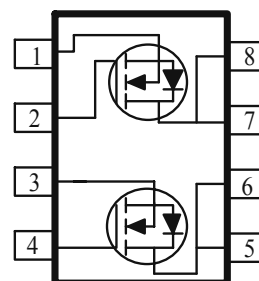
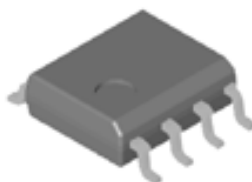


## Dual N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
20	58 @ $V_{GS} = 4.5V$	5.0
	82 @ $V_{GS} = 2.5V$	4.2



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	5.0	A
	$T_A = 70^\circ\text{C}$		4.1	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 30$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	1.7	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.1	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
	Steady State		80	$^\circ\text{C/W}$

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

**SPECIFICATIONS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	0.7			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 16\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}$ , $V_{GS} = 4.5\text{ V}$	20			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$			58	m $\Omega$
		$V_{GS} = 2.5\text{ V}$ , $I_D = 4.2\text{ A}$			82	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 5\text{ A}$		22		S
Diode Forward Voltage	$V_{SD}$	$I_S = 1.7\text{ A}$ , $V_{GS} = 0\text{ V}$		0.7		V
Dynamic <sup>b</sup>						
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$		7.5		nC
Gate-Source Charge	$Q_{gs}$			0.6		
Gate-Drain Charge	$Q_{gd}$			1.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ , $I_D = 1\text{ A}$ , $V_{GEN} = 4.5\text{ V}$		22		nS
Rise Time	$t_r$			40		
Turn-Off Delay Time	$t_{d(off)}$			50		
Fall-Time	$t_f$			20		
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{S}$		40		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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