# N-Channel 250-V (D-S) MOSFET

# **Key Features:**

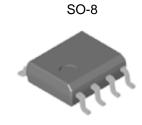
- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- · Fast switching speed

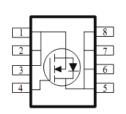
Typical	l Applica	ations:
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- · White LED boost converters
- · Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$r_{DS(on)}(\Omega)$	I <sub>□</sub> (A)	
250	1.6 @ V <sub>GS</sub> = 10V	1.2	
	$1.8 @ V_{GS} = 6V$	1.1	







ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		$V_{DS}$	250	V	
Gate-Source Voltage			±20	V	
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	· I <sub>D</sub>	1.2		
Continuous Drain Current	T <sub>A</sub> =70°C	'D	1	Α	
Pulsed Drain Current <sup>b</sup>			5		
Continuous Source Current (Diode Conduction) a			3.7	Α	
Dower Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	$P_{D}$	3.1	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	' D	2.2	VV	
Operating Junction and Storage Temperature Range		$T_J$ , $T_{stg}$	-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\theta JA}$	40	°C/W		
Maximum Junction-to-Ambient	Steady State	IΛθJA	80	C/VV		

1

#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

### **Electrical Characteristics**

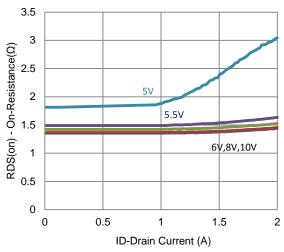
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	1	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Brain Current	I <sub>DSS</sub>	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	1.8			Α	
Drain Cauras On Basistanas a	r	$V_{GS} = 10 \text{ V}, I_{D} = 1 \text{ A}$			1.6	Ω	
Drain-Source On-Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 0.8 \text{ A}$			1.8	22	
Forward Transconductance a	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 1 \text{ A}$		3		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.8 \text{ A}, V_{GS} = 0 \text{ V}$		0.82		V	
		Dynamic <sup>b</sup>					
Total Gate Charge	$Q_g$	$V_{DS} = 100 \text{ V}, V_{GS} = 6 \text{ V},$		3			
Gate-Source Charge	$Q_{gs}$	$I_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$ $I_{D} = 1 \text{ A}$		1.3		nC	
Gate-Drain Charge	$Q_{gd}$	10 = 1 A		1.4			
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DS} = 100 \text{ V}, R_{L} = 100 \Omega,$		6			
Rise Time	t <sub>r</sub>	$V_{DS} = 100 \text{ V}, K_L - 100 \Omega,$ $I_D = 1 \text{ A},$		5		no	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		14		ns	
Fall Time	t <sub>f</sub>	VGEN = 10 V, NGEN = 0 12		6			
Input Capacitance	C <sub>iss</sub>			248			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		30		pF	
Reverse Transfer Capacitance	$C_{rss}$			11			

#### Notes

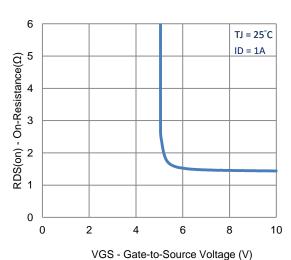
- Pulse test: PW <= 300us duty cycle <= 2%.
- Guaranteed by design, not subject to production testing. b.

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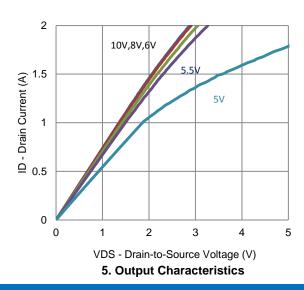
# **Typical Electrical Characteristics**

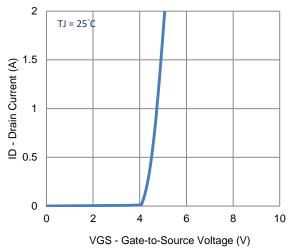


#### 1. On-Resistance vs. Drain Current

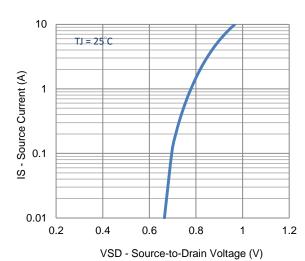


3. On-Resistance vs. Gate-to-Source Voltage

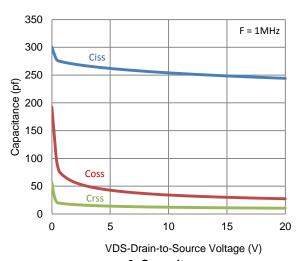




2. Transfer Characteristics

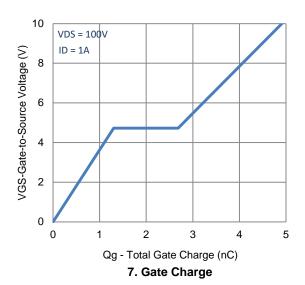


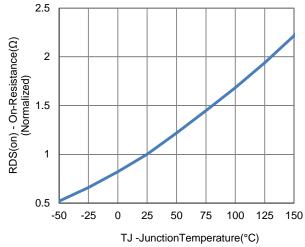
4. Drain-to-Source Forward Voltage



6. Capacitance

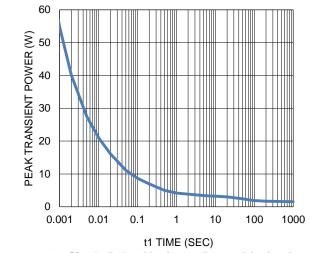
# **Typical Electrical Characteristics**





10 us
10 us
100 us
100 us
100 ms

8. Normalized On-Resistance Vs Junction Temperature



VDS Drain to Source Voltage (V)

9. Safe Operating Area

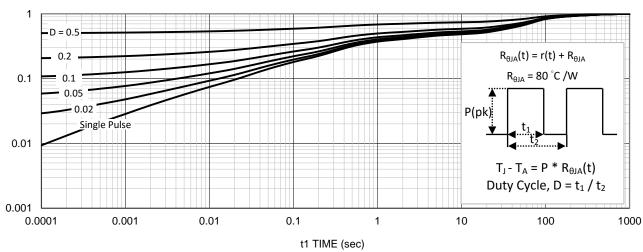
100

1000

10000

10

10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

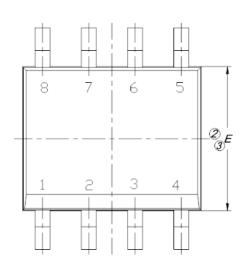
ID Current (A)

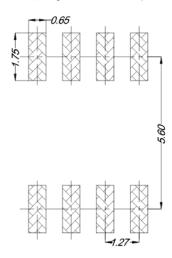
0.01

0.1

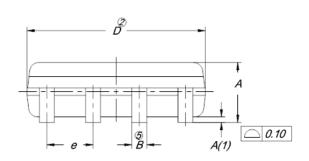
### **Package Information**

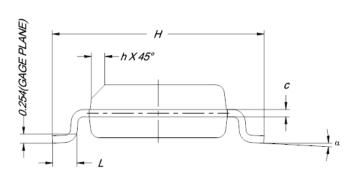
Land Pattern (Only for Reference)





DIM.	MILLIMETERS				
	MIN.	NOM.	MAX.		
Α	1.35	1.55	1.75		
A(1)	0.10	0.18	0.25		
В	0.38	0.45	0.51		
С	0.19	0.22	0.25		
D	4.80	4.90	5.00		
E	3.80	3.90	4.00		
е	1.27 BSC				
Н	5.80	6.00	6.20		
L	0.50	0.72	0.93		
α	0°	4°	8°		
h	0.25	0.38	0.50		





#### Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.