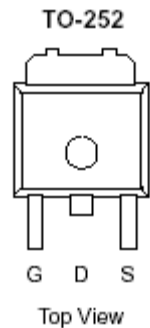
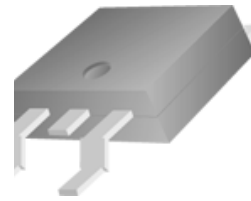


N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
100	28 @ $V_{GS} = 10V$	35
	30 @ $V_{GS} = 4.5V$	33

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_C=25^\circ\text{C}$ I_D	35	A
Pulsed Drain Current ^b	I_{DM}	36	
Continuous Source Current (Diode Conduction) ^a	I_S	30	A
Power Dissipation ^a	$T_C=25^\circ\text{C}$ P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C}/\text{W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	34			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$			28	m Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 1 \text{ A}$			30	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 40 \text{ V}$, $I_D = 1 \text{ A}$		4.4		S
Diode Forward Voltage	V_{SD}	$I_S = 1 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.1		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 25 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$		30		nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}$, $R_L = 25 \Omega$, $I_D = 9 \text{ A}$, $V_{GEN} = 10 \text{ V}$		10		nS
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(off)}$			90		
Fall-Time	t_f			20		

Notes

- Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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