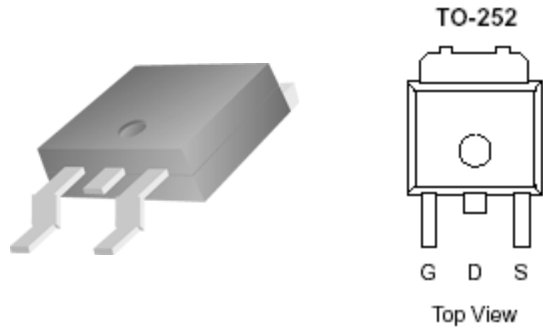


**P-Channel 20-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range ( $\pm 25$ ) for battery pack applications

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (mΩ)	I <sub>D</sub> (A)
-20	118 @ V <sub>GS</sub> = -4.5V	17
	178 @ V <sub>GS</sub> = -2.5V	14



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V <sub>DS</sub>	-20	V
Gate-Source Voltage		V <sub>GS</sub>	±12	
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	I <sub>D</sub>	17	A
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	±40	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	-30	A
Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	P <sub>D</sub>	50	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	50	°C/W
Maximum Junction-to-Case	R <sub>θJC</sub>	3.0	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

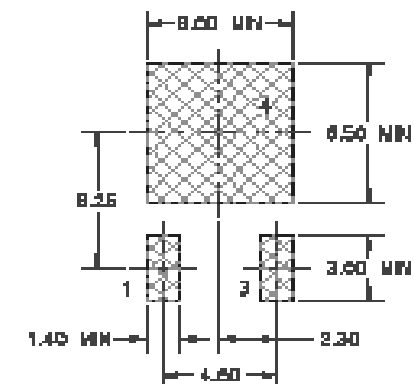
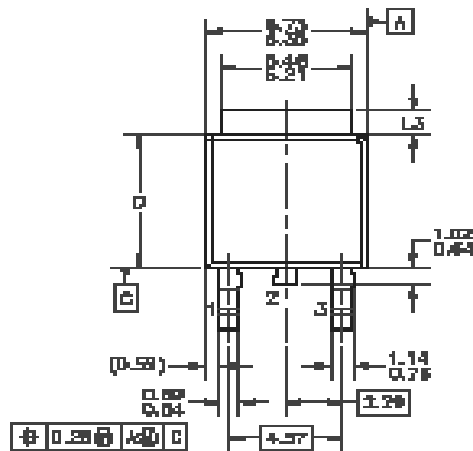
SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.7			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-41			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -17 \text{ A}$			118	m $\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -14 \text{ A}$			178	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = -10 \text{ V}, I_D = -17 \text{ A}$		31		S
Diode Forward Voltage	$V_{SD}$	$I_S = -41 \text{ A}, V_{GS} = 0 \text{ V}$		-0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -21 \text{ A}$		12.2		nC
Gate-Source Charge	$Q_{gs}$			1.1		
Gate-Drain Charge	$Q_{gd}$			1.5		
<b>Switching</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 15 \Omega, I_D = -41$ $\text{A}, V_{GEN} = -4.5 \text{ V}, R_G =$ $6 \Omega$		15		nS
Rise Time	$t_r$			12		
Turn-Off Delay Time	$t_{d(off)}$			62		
Fall-Time	$t_f$			46		

## Notes

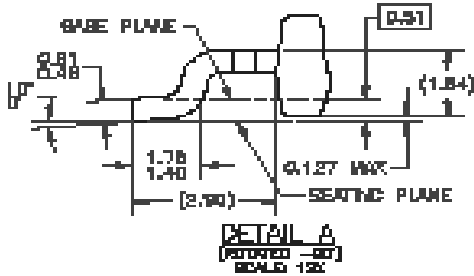
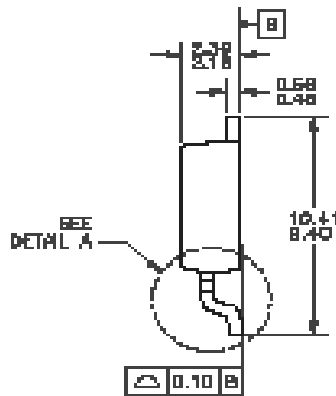
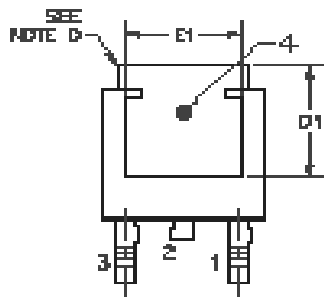
- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.43-0.49
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.37 MIN