Thermal Performance of MOSFET DFN Packages

The use of DFN style packages for Power MOSFETs is an obvious extension of the widespread use of QFN packages for ICs, and brings smaller yet thermally superior packages for MOSFETs. It takes advantage of advances in silicon that have facilitated smaller die for a given on-resistance, and creates an extensible family rather than looking for the next smallest existing package in the market as silicon performance increases. However thermal data from vendors is hard to apply to real life conditions, with data sheets giving a number for use mounted on a one inch square PC Board, which may or may not reflect use on a practical PC Board. Analog Power has characterized a variety of packages and boards to provide some real data and understanding of the thermal properties; the intent is to show data here that will be close to most actual PC Boards. The DPAK and SO-8 were included in the data to allow comparison with these packages.

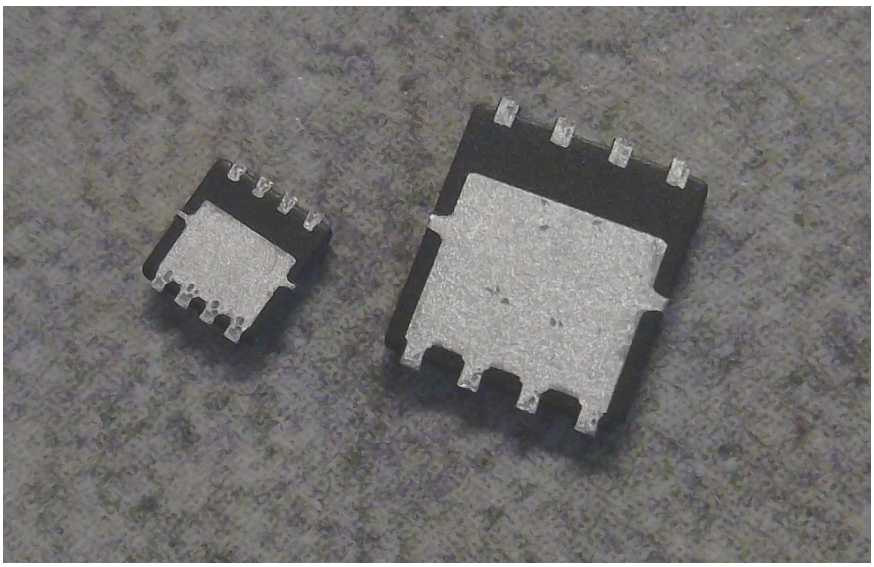

Figure 1. DFN3x3 and DFN5x6 (SOIC-8 Footprint) Packages

Even the same die on the same PC board will exhibit different thermal behavior in different sized DFN packages. Unless a heatsink is attached to the top of the package, the heatsink for surface mount packages is the PC board itself and the thermal impedance from the die to the PC board should be a small component of the total thermal resistance for an exposed pad DFN package. What is critical, however, and varies from package to package, is the resistance due lateral spreading of the heat around the package thermal effective footprint (i.e. exposed drain connection. The copper tab of a package has lateral thermal conductivity much greater than a PC board; a larger copper tab periphery results in lower thermal impedance. The use of ground planes and four-layer boards provides another thermal path, which also assists in spreading, however the heat must first pass through the laminate, and smaller copper-footprints will mean that the impedance to another plane is higher due to the small area. Figure 2 illustrates a simple breakdown of the components of junction to ambient thermal impedance and shows the

leadframe footprint and area component which is dependent on the package size. There are of course many different levels of detail possible for this breakdown, for example die attach could be included, etc.

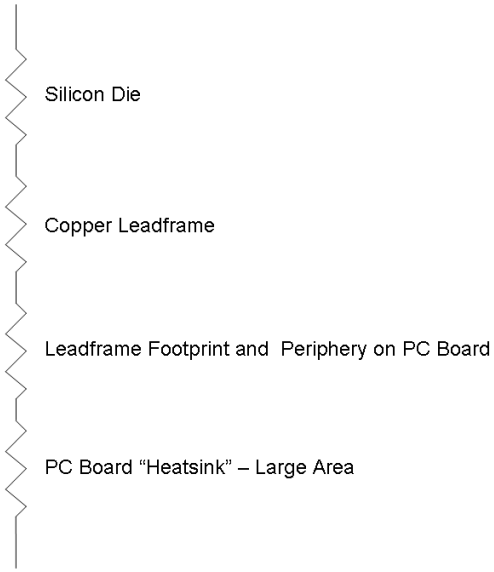

Figure 2. Breakdown of Thermal Impedance Showing Periphery Impedance

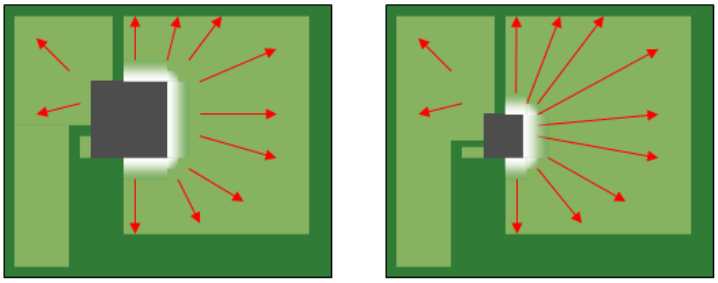

Figure 3. Effect of Package Size on Thermal Impedance Due to Periphery

Larger packages have larger periphery which improves transfer to the large area of the PC board "heatsink" and reduces thermal impedance

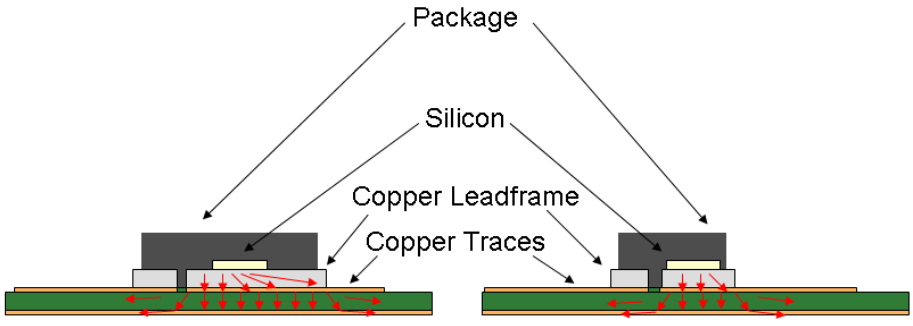

Figure 4. Effect of Package Size on Transfer Through PC Board

Larger packages have more leadframe area which helps spread the heat and improve transfer to the PC board and other copper layers

Most data sheets show thermal impedance limit when mounted on a one inch by one inch PC Board, which is not going to be 100% representative of a real-life board. A more useful number may be when mounted on a large PC board with at least one inch by one inch copper fill on the drain and a ground plane. It is not well documented how much effect ground planes and copper fills have on thermal properties, however copper close to the device can only help thermally. In most cases where thermal properties matter, the electrical connections to the drain and source require copper fills, so the copper that is required for electrical connection is available for thermal conduction and greatly assists in spreading, although FR4 laminate does also conduct some heat. In this application note we take data with minimal copper near the device and with significant copper fills. In all cases we assume a ground plane is present.

Thermal Impedance Measurement Methodology

Steady state thermal impedance was measured using the change in the V_{SD} of the body drain diode at a low current after heating the device for a significant time using the internal diode at a higher current[1]. By ensuring the device is at steady state temperature, the power dissipation is also steady state and voltage over and current through the device can be measured accurately.

The low current through the diode was applied via a 9-V power supply and a resistor. The resistor value shown is for large MOSFETs and a higher value is used for smaller die to ensure similar K factors. The forward voltage of the diode was measured and recorded on a digital storage 'scope. A heating current was then applied from a power supply and the board left for at least ten minutes to reach equilibrium. After ten minutes, the heating voltage and current were recorded. With the scope triggering off the diode voltage, the heating current was removed and the waveform of the diode voltage captured. The V_{SD} of the diode a few microseconds after power was removed is easily read and the delta V_{SD} due to the known power applied derived.

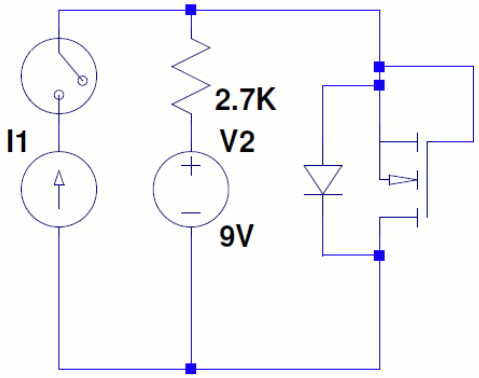

Figure 5. Schematic for Thermal Testing. Heating Power Source is Drawn as a Current Source.

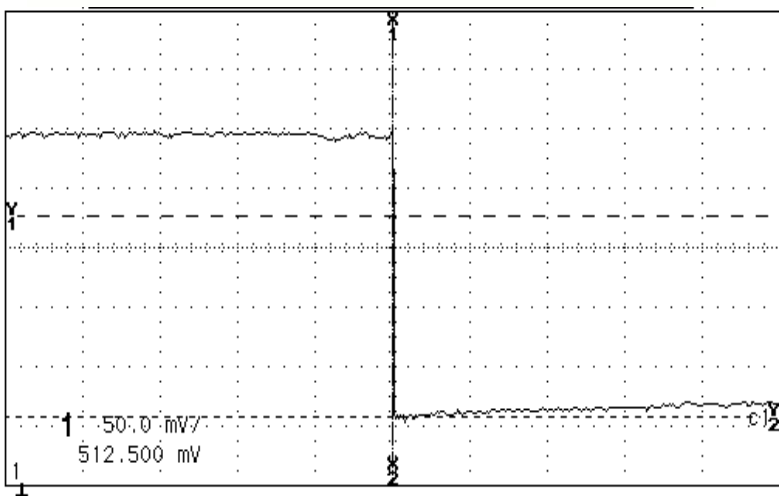

Figure 6. V_{SD} Waveform When Heating Power is Removed. Cursor Y1 is the recorded V_{SD} of the diode at room temperature. The second cursor is then set to the minimum V_{SD} observed as shown. The scope then provides the delta V_{SD}.

Two large ground plane boards were tested, 25 mm x 25 mm and 10 mm x 15 mm Drain copper fills. The former used 25 mm (1-inch) square copper fills for the Drain and 20 mm x 25 mm fills for the Source. The other board used 10 mm x 15 mm fills for the Drain and normal traces for the Source. Both boards had a copper ground plane on the opposite side from the components.

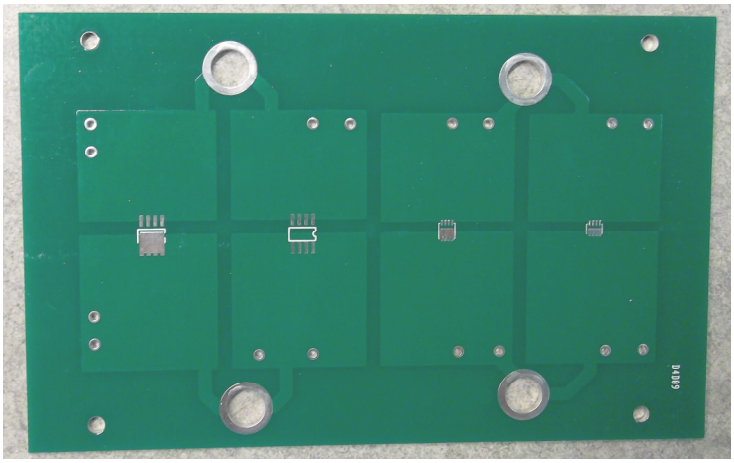

Figure 7a. Actual 25 mm Top Copper Test Board

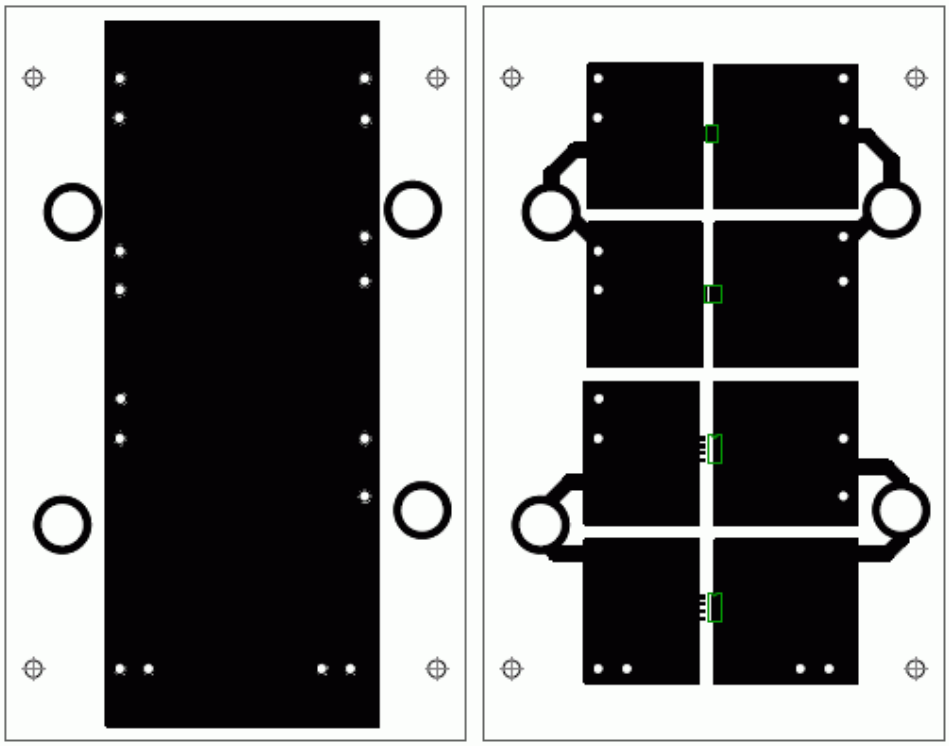

Figure 7b. 25 mm Test Board Layout Top and Bottom Copper Artwork

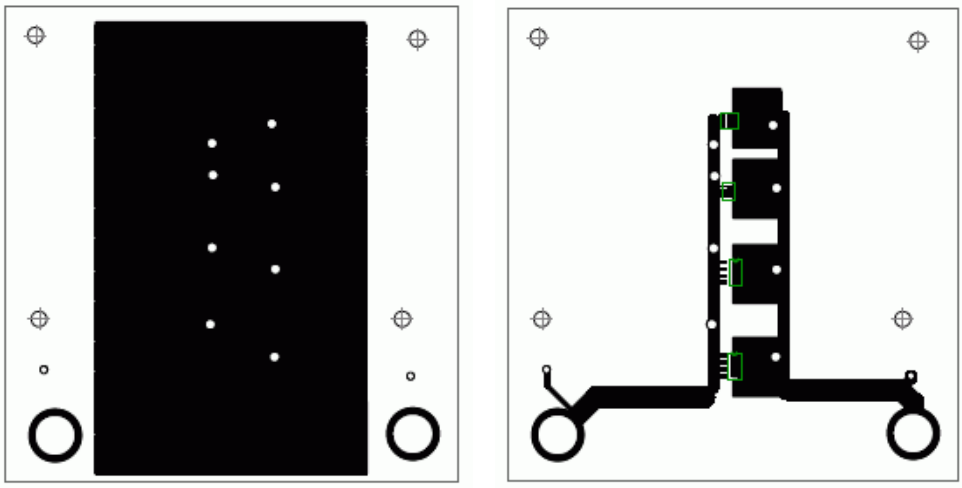

Figure 8. 10 mm x 15 mm Test Board Layout (same scale as Figure 7)

Results: DFN2x3, DFN3x3, DFN5x6, SO-8, DPak

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN2x3	10 mm x 15 mm	0.58	71.9	50.9
		1.07	130	50.8
		1.61	201.5	52.1
		Average		51.3
	25 mm x 25 mm	0.82	59.4	46.2
		1.81	131.2	48.0
		2.40	171.8	48.9
		Average		47.7

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN3x3	10 mm x 15 mm	0.64	72	44.9
		1.07	125	46.6
		1.33	156.2	47.0
		Average		46.2
DFN3x3	25 mm x 25 mm	1.03	60.5	39.0
		2.02	117.2	39.6
		2.92	165.6	39.8
		Average		39.5

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN5x6	10 mm x 15 mm	0.98	37.5	38.2
		1.29	121	39.1
		1.79	168.5	39.2
		Average		38.8
	25 mm x 25 mm	0.8	63	32.6
		1.30	103.1	33.1
		1.85	145.3	32.7
		Average		32.8

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
SO-8 (for comparison)	10 mm x 15 mm	0.98	123.4	52.5
		1.36	170.3	52.4
		1.70	214	52.5
		Average		52.4
	25 mm x 25 mm	0.67	73.7	46.0
		1.28	141.4	46.1
		1.79	199.1	46.4
		Average		46.2

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DPAK (for comparison)	25 mm x 25 mm	0.67	42.2	28.7
		1.31	82	28.5
		1.86	53.3	28.5
		Average		28.6

Summary of Results

Package	Observed RTHJA	
	10 mm x 15 mm board	25 mm x 25 mm board
DFN2x3	51.3°C/W	47.7°C/W
DFN3x3	46.2°C/W	39.5°C/W
DFN5x6	38.8°C/W	32.8°C/W
SO-8	52.4°C/W	46.2°C/W
DPAK	-	28.6°C/W

Note: all values shown here are numbers derived from limited experimental data and must not be used as limits for design purposes. Actual performance is very dependent on PC Board characteristics; boards used for testing were 1 oz copper. Performance of each package relative to the others shown can be considered reasonably accurate, however.

Performance of DFN2x2 and TSOP-6 Packages

Analog Power has recently introduced a line of MOSFETs in a DFN2x2 package:

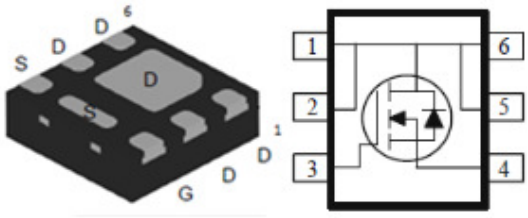

Figure 9. DFN2x2 Package

These packages have an effective drain-footprint of about 1.3 x 2 mm, compared with a DFN2x3 (as tested in the first part of the application note) of 2.3 x 1.15 mm and a DFN3x3 of 2.3 x 2.3 mm. Since the area and periphery are key factors in heat flow to the PC board and then to ambient, we would expect the DFN2x2 to be slightly higher thermal impedance than the DFN2x3 given its area is about the same, but periphery slightly smaller.

To evaluate the DFN2x2 and TSOP-6 a new, individual, board was made. A DFN5x6 version of the new board was also made to calibrate the board against the first board shown in Figure 7, which has a ground plane 120mm x 50 mm. Since the new boards are individual/single package boards, the board itself is only 38 mm x 38 mm, so the board has a significantly smaller ground plane, 33 x 33 mm.

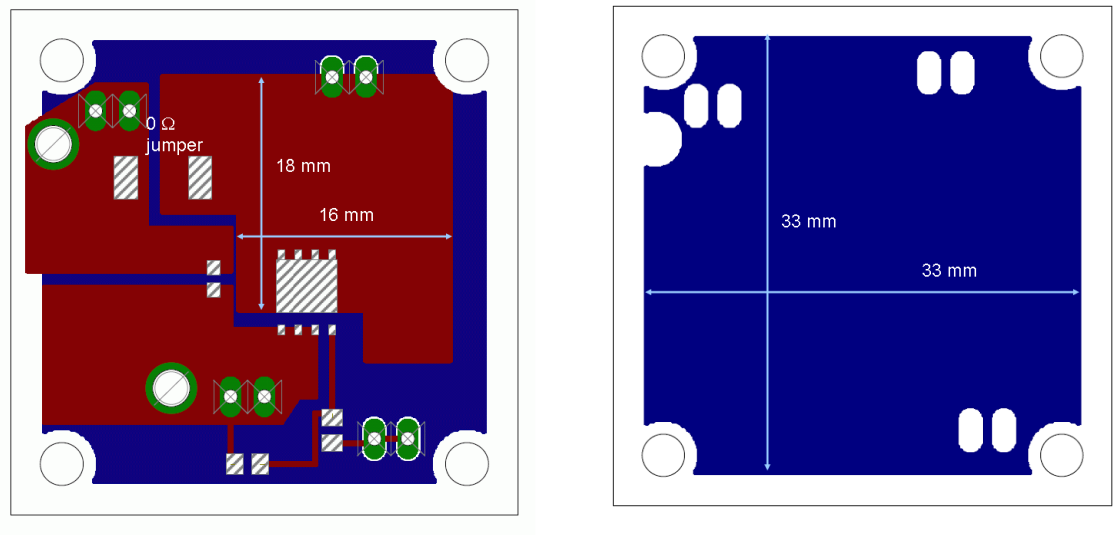

Figure 10. Test Board Layout (DFN5x6 shown, 18 mm x 16.mm Top copper plane, 33 x 33 mm bottom copper plane. The board outline is 38 mm x 38 mm.

The DFN2x2, TSOP-6 and DFN5x6 were tested on this board in the same manner as shown in Figures 5 and 6.

RTHJA Results

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN2x2 (AMA430N)	Drain:18 x 16 mm Gnd Plane: 33 x 33 mm	0.72	85.7	59.5
		1.08	129	59.8
		1.66	198	59.7
		Average		59.7

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
TSOP-6 (AM3402N)	Drain:18 x 16 mm Gnd Plane: 33 x 33 mm	0.74	96.9	65.4
		1.39	184	66.1
		1.63	215	66.1
		Average		65.9

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN5x6 (AMR438N)	Drain:18 x 16 mm Gnd Plane: 33 x 33 mm	0.93	88.0	44.7
		1.23	1116	44.9
		1.70	162	45.4
		Average		45.0

Comparing this board with the multi-package board using the DFN5x6 as a reference we see:

Board	Thermal Impedance, RTH (°C/W)
Drain: 25 x 25 mm, Plane: 120 x 50 mm	32.8
Drain: 10 x 15 mm, Plane: 80 x 50 mm	38.8
Drain: 18 x 18 mm, Plane: 33 x 33 mm	45.0

This is as expected, and emphasizes the effect of both drain copper fill area and ground plane. In most boards a very large ground plane is possible as it will be a full layer the whole area of the board.

In order to further investigate the effect of the amount of copper present on boards, a slightly smaller version of the board was used for a second single-device evaluation. The TSOP-6 version is shown here; the DFN2x2 and DFN5x6 boards have the same size copper planes.

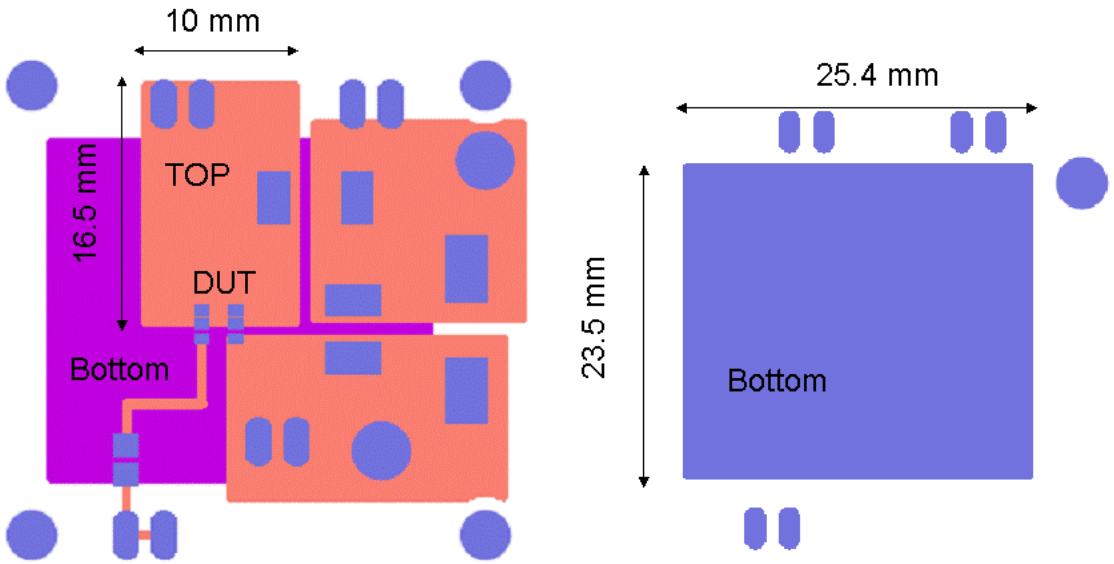

Figure 11. Smaller Ground Plane Test Board Layout (10 mm x 16.5mm Top copper plane, 25.4 x 23.5 mm bottom copper plane. The board outline is 38 mm x 38 mm.

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN2x2	T: 10 mm x 16.5 mm B: 23.5 mm x 25.4 mm	1.312	191	68.5

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
TSOP-6	T: 10 mm x 16.5 mm B: 23.5 mm x 25.4 mm	1.01	147	76.2

Package	Layout	Power (W)	Delta VSD (mV)	RTH (°C/W)
DFN5x6	T: 10 mm x 16.5 mm B: 23.5 mm x 25.4 mm	1.59	181	53.5

The DFN5x6 data shows that this board layout is worse thermally than the larger board and even more dramatic difference compared with a much larger ground plane on the bottom of the board as used for the original thermal impedance measurements. The original board showed a thermal impedance of 38.8°C/W, compared to the 53.5°C/W seen here for the same drain area. Note that the TSOP-6 has impressive performance. This is due to the fact that the package has four drain leads, one at each corner of the drain leadframe. This allows a short effective path for the heat and increases the footprint periphery compared to say 4 drain leads on one side.

Conclusion

The data show that impressively low thermal impedance numbers can be seen using very small surface mount packages. Even the DFN2x3 has similar performance to the SO-8 package.

Increasing the amount of copper around the drain does make a difference, but the difference between 150 mm^2 and 625 mm^2 is not as large as may be expected, as long as another layer has extensive solid copper such as a ground plane. The large board showed a thermal impedance of 38.8 °C/W, but the smallest board tested with similar drain copper fill, but ground plane 23.5 mm x 25.4 mm, approximately 1 square inch, was 53.5 ° C/W.

As has been shown in previous data[2], the DFN5x6 will have a thermal impedance approximately 15 °C/W better than an SO-8 package, assuming a reasonable amount of local copper on the PC Board. The DPAK has slightly better performance than the DFN5x6 due to the larger, thicker copper paddle (5.3mm x 4.4 mm compared with 3.6 x 4.3 mm providing more heat spreading within the package.

The smaller DFN packages, namely DFN2x2 and DFN 3x3 have an impressive thermal performance. With a full layer ground plane and ~15mm x 20mm drain fill, typical thermal impedances of <60°C/W should be possible even for a DFN2x2 package.

The TSOP-6 has impressive thermal performance for its size, and is only a little worse then the SO-8. Its high performance for a small leaded package is due to the fact that heat is carried by four leads at each corners of the drain leadframe.

References

1. “MOSFET Thermal Characterization in the Application”, Vishay Siliconix AN819, 2001
2. “Thermal Ratings for Analog Power Surface Mount MOSFETs”, Analog Power AN2008-1, 2008