Thermal Ratings for Analog Power Surface Mount MOSFETs

Thermal ratings for surface mount MOSFETs and the ratings derived from them are sometimes a source of confusion. Semiconductor manufacturers have struggled to provide ratings that both accurately represent the device and yet are realistic for the device mounted on a PC board, two different aspects that are, to some extent, mutually exclusive. This article explains the ratings on Analog Power data sheets and how to use them.

The first standard surface mount package for power transistors was the DPAK. It was initially rated using T_{case} = 25°C, an impossible condition for real applications, and therefore not useful to calculate real current ratings. When MOSFETs were introduced in the SO-8 package, vendors broke with that hypothetical rating and attempted to show a much more usable thermal rating. The intent was to show a realistic rating for maximum power dissipation, but the dilemma was that the true rating depended on the printed circuit board as much as the device. The ratings shown on the first data sheets were optimistic for a standard PC board as they focused on the device, not the PC board, but were possible to attain if sufficient heat sinking was available through the board. Today data sheets typically show a ten-second pulse maximum power dissipation which can be attained on a PC board with standard high current traces. For such a pulse the copper on the printed circuit board does not reach steady-state, so it is a rating that partially describes the device, and partially the board. A value is usually also given for steady-state thermal impedance, junction-to-air while mounted on a one inch square board. This number depends on the PC board as much as the product the vendor is producing. Since few applications use solid copper areas connected to the drain, it is not a practical number, but is still very useful.

The steady-state maximum junction-to-ambient thermal impedance is shown on Analog Power data sheets for devices mounted on a one-inch by one-inch FR4 board. It is really a best case number, as not many applications allow the use of so much copper, however being a maximum rating, there is some margin over typical numbers. The specification shown on the Analog Power data sheets is a reasonably accurate representative of the total system if a ground plane or similar is present on the PC board, and some additional copper (compared with standard logic layouts) is used near the drain connections,. It should be noted that these ratings are not truly device ratings, they are characteristics of a piece of PC board material as much as they are characteristics of the MOSFET. It can be seen that a key factor in reducing thermal impedance is the number of drain leads the package provides, the SOT-23 being a poor thermal performer due to the single drain lead.

Package	Number of drain leads	Steady-State, 1 inch x 1 inch FR4 board	
		Maximum Thermal Impedance	Corresponding Max. Power Dissipation
DPAK	-	50 °C/W	2.5 W
SO-8	4	80 °C/W	1.6 W
SO-8 (lead-less)	-	65 °C/W	1.9 W
SOT-23	1	166 °C/W	0.75 W
DFN3x3	-	81 °C/W	1.5 W
DFN2x2	-	90 °C/W	1.4 W
TSOP-6	4	110 °C/W	1.14 W
TSSOP-8	3	115 °C/W	1.1 W

Table 1. Steady State Thermal Impedance Ratings and Corresponding Power Dissipation Ratings for Analog Power's Surface Mount MOSFET Packages.

Since these thermal impedance numbers are PC board dependent, they are affected by the amount of copper close to the device. The accuracy depends on just how much copper is present. Smaller packages tend to be more limited in this respect, but that is, to some extent, included in the rating. For a practical optimized layout, the area underneath the device should be copper connected directly to the drain pin, and there should be as much copper as possible close to the drain pin(s). Since these numbers represent best case thermal impedance/power dissipation, some additional de-rating should also be applied to allow for a realistic PC board and the design tested thermally before production. As long as the area under the package is connected to the drain lead, wide traces are used close to the drain, and there is a ground plane in the PC board, very little, if any, additional de-rating need be applied. The fact that the data sheet number is a maximum, as opposed to a typical number, provides some inherent de-rating

The transient thermal impedance curve for surface mount MOSFETs is a useful tool to help understand the realities of thermal impedance. The curve clearly shows that steady state equilibrium is not reached until over 200 seconds, hence we define steady-state in this context as t > 500 seconds. This long time constant reflects the copper on the PC board, not the device. For an SO-8, the effective thermal impedance for a 10 second pulse is approximately half the steady-state value, assuming a reasonable amount of copper is present, either connected to the drain or as a ground plane.

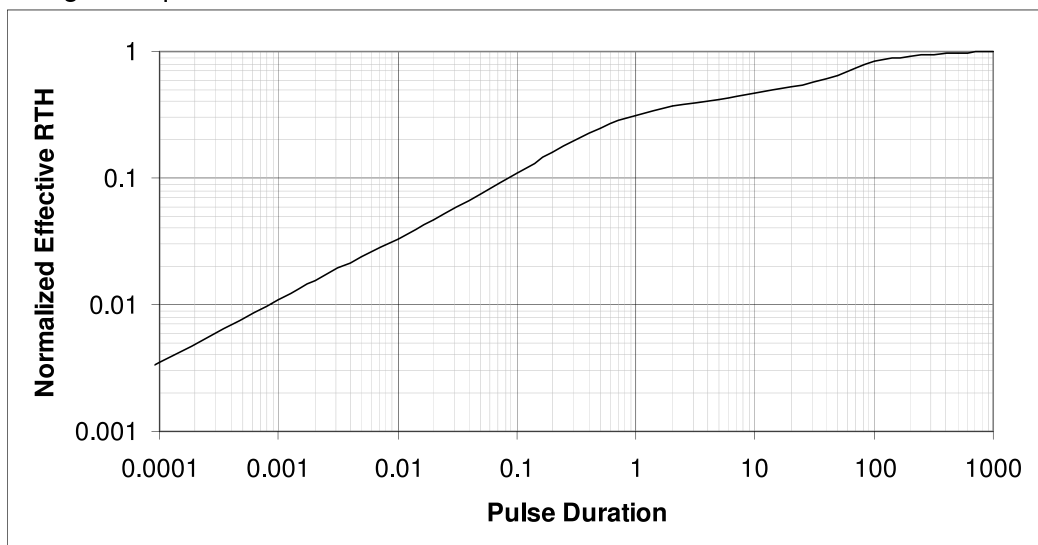


Figure 1. Transient Thermal Impedance Curve for a Power MOSFET in an SO-8 Package

It may be confusing as to which value is used for the base (t = infinity) for the transient thermal impedance curve, is it the specification/limit or the typical? Since the curve always tends to Z_{TH} = 1.0, it shows that the curve is normalized to the actual steady-state value for the device tested. It can, however, also be applied to the maximum limit to give a fairly reliable limit for transient thermal impedance at different pulse durations.

Absolute maximum steady-state current ratings for surface mount MOSFETs are calculated from the 10-second maximum power dissipation, which is actually much more realistic then the TO-220 practice of assuming an infinite heat sink (I.E. T_{case} = 25°C.) Note that absolute maximum ratings of this type are applied simultaneously and no single rating may be exceeded. The maximum junction temperature is the limiting rating, so arguably the continuous drain current rating is irrelevant as an

absolute maximum, but is included as a useful reference. The user should ensure that the maximum junction temperature is not exceeded (normally de-rating is also applied) and the maximum continuous current is a different, higher limit which can usually be ignored. Even the term “continuous” is ambiguous, in some systems a ten second pulse would be considered continuous. In any case the industry standard has evolved that a MOSFET rated at 10-Amp on the datasheet will typically be used at a lower continuous current if mounted on a standard PC board with no forced air cooling. The critical limit is the junction temperature and the issue is to calculate and/or measure the junction temperature for a given MOSFET under the conditions.

Junction temperature is best estimated using a thermocouple on the foot of a drain lead, assuming the thermal impedance from that point to the chip is approximately 80 °C/W per drain lead using the chip power dissipation (as opposed to the heat flow per lead.) The applicable value for an SO-8 is therefore 20 °C/W based on four drain leads and the chip’s power dissipation. An infra-red thermal probe measuring the case temperature will give a number approximately equal to the lead temperature, but is not practical for smaller packages. Junction temperature can also be estimated by measuring the temperature of the plastic surface of the case and adding 5% to 10% of the measured value of the temperature rise (over ambient) to compensate for the temperature drop through the plastic. This method relies on the fact that the heat flow through the case as opposed to through the copper leadframe is minimal.

Surface mount MOSFETs are limited in their steady-state current handling capability compared with TO-220 packages by their small heat sink, the PC board. However, for short pulses and even pulses of the order of one second they compare favorably with devices in more traditional packages. The result is a pulse-current capability far greater than the steady state capability. For example looking at the AM4874N MOSFET, the transient thermal impedance for a 0.1 second pulse is about ten times the ten-second value, which gives more than three times the data sheet current rating capability. Such inrush-type surges are common in many applications using surface mount MOSFETs, and this extra capability means such MOSFETs usually do not need to be oversized for inrush and surges, meaning a smaller MOSFET will suffice.

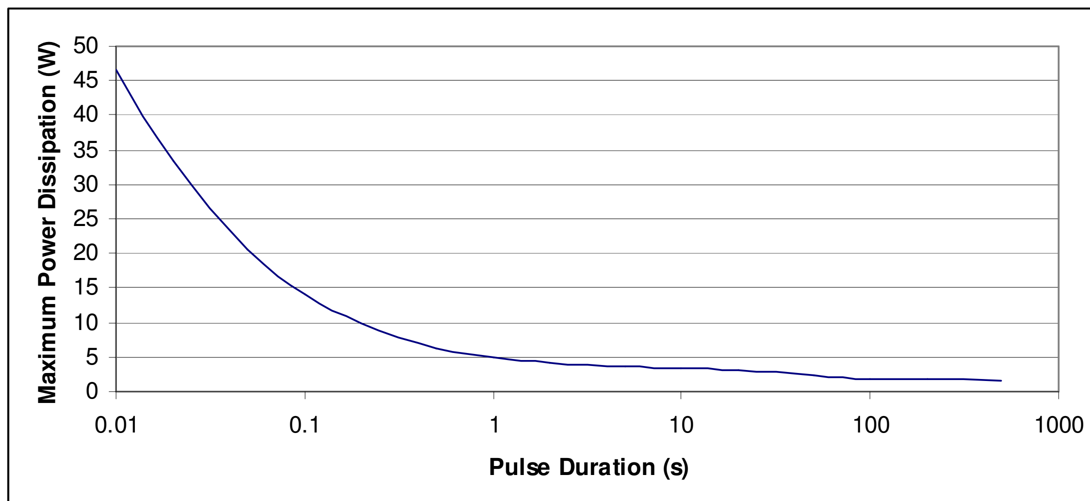


Figure 2. Maximum Power Dissipation vs. Pulse Duration

One major ambiguity remains: how are packages containing two MOSFETs rated? The manufacturers were presented with a dilemma as there are a range of applications and associated thermal systems. The industry standard, which has been adopted by Analog Power, is to show thermal impedance and resulting maximum power dissipation for one of the two devices using a

ten-second pulse rating. Being a ten-second pulse rating, this really reflects the package more than the total system, so how much heat the other co-packaged device is generating is not relevant, at ten seconds the heat has not spread significantly on the PC board and the two devices do not interfere with each other thermally. In an actual application, the two MOSFETs share a heat sink (the PC board), so the operation of one MOSFET does affect the other. Data sheets do also show steady-state thermal impedance for each device, and this value is higher than a single device, but not double, and assumes no “interference” (I.E. effect from sharing a heat sink) from the other co-packaged MOSFET, which may not be practical. Therefore for packages containing two MOSFETs which both dissipate significant heat, additional de-rating (compared with a single device) from the steady state value on the data sheet may be required.

Two MOSFETs packaged in a TSOP-6 (also known as a dual) is a particularly poor package for power dissipation when compared with the single MOSFET in the same package. In a single MOSFET device, 4 leads are used to connect to the drain and hence used to conduct and spread heat. In a dual MOSFET configuration, only one lead is used for each drain, increasing thermal impedance and reducing heat spreading. Therefore in a TSOP-6 dual, the total maximum power dissipation of the two MOSFETs will be less than that of a single in the same package. With a higher lead count, the Analog Power DFN3x3 package solves this problem and provides a direct heat flow path for each drain (which is the main heat flow path). This exciting package is capable of superior electrical performance than the TSOP-6, has a similar footprint and has dramatically better thermal performance.

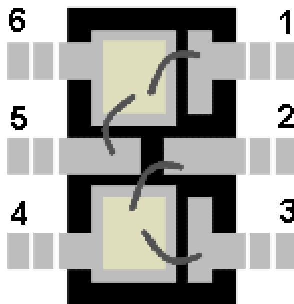


Figure 3. Dual TSOP-6 MOSFET
One lead carries heat from each die

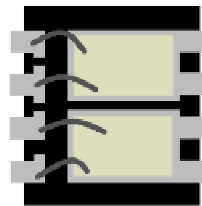


Figure 4. Dual DFN3x3
Heat carried vertically from each die to board

Another design that can be used to improve the thermal performance of dual MOSFET devices is to use a common (I.E. connected) drain pad, such as in the AM4520H. This device consists of a complementary N- and P-Channel MOSFET in an SO-8 package but with a common drain connection as used in bridge circuits. Such a configuration improves the thermal impedance significantly where one device generates significantly more heat that the other, which is a common circumstance given different polarity and switching characteristics.

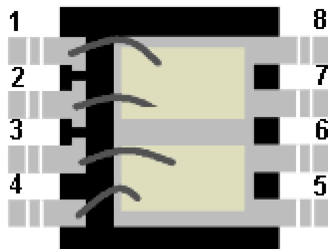


Figure 5. Common Drain Package. Using a common drain, the thermal impedance of the AM4520H is improved compared with separate drain connections, assuming the two die dissipate different powers.

Some manufacturers now provide “junction-to-foot” thermal impedance ratings. One manufacturer provides the same figure but calls it “junction-to-case” and defines “case” in this context as the mounting surface of the drain leads. Such numbers would have some use to calculate total junction to ambient temperatures if the exact thermal impedance of the PC board (taking into account each lead/individual heat source) could be calculated and if the exact losses in the MOSFET are known. In reality both figures are very hard to calculate, so the junction-to-foot thermal impedance is of little practical use. One side effect of providing a junction-to-foot or junction-to-case thermal impedance is that the manufacturer can state that the junction-to-case thermal impedance is a function of the device, but junction-to-ambient thermal impedance is a function of the user’s board, which is a valid point.

Analog Power also produces MOSFETs in the lead-less SO-8, referred to as PowerPak by Vishay Siliconix. This package provides a direct path for the heat from the die to the PC board, without relying on leads to carry heat. This is a good example of where junction-to-case type thermal impedance can be used to distinguish packages, yet has a smaller than expected impact on the total system.

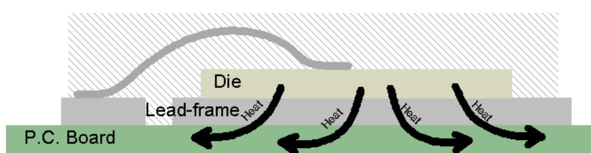


Figure 6. Lead-less SO-8 Heat Flow

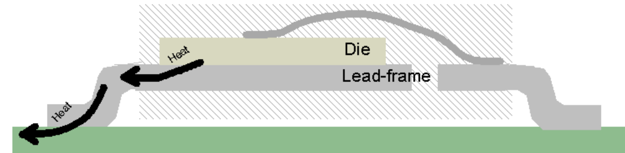


Figure 7. SO-8 Heat Flow

Package	Actual Thermal Impedance			
	Junction-to-case	Junction-to-ambient		
		On Copper*	Typical**	Minimal**
SO-8	20 °C/W	60 °C/W	80 °C/W	125 °C/W
Lead-less SO-8	1.8 °C/W	45 °C/W	65 °C/W	Not Applicable

* performance where soldered directly to ground or power plane, >1 square inch exposed copper.
** “Typical” and “Minimal” refer to typical power PC board layout and minimal amounts of copper adjacent to the drain connection. These numbers assume a ground plane is present.

Table 2. Comparison of SO-8 and lead-less SO-8.

Note that the lead-less SO-8, despite having one tenth the junction-to-case thermal impedance, has only about 20% improvement in thermal impedance when mounted on a typical PC board. However, when mounted directly on a large area of exposed copper, as may be the case in a high current dc/dc converter, the percent advantage over the SO-8 is much higher. Since on-resistance increases with junction temperature, a lower junction temperature actually reduces the on-resistance if everything else is equal, increasing the electrical efficiency. Therefore the lead-less SO-8 shows a large increase in performance when used in circuits such as high power DC/DC converters where large areas of copper are present, and is the package of choice for such circuits.

Typically the most important parameter in the thermal design is the steady-state thermal impedance, junction-to-air. Some manufacturers publish Spice thermal models for their devices, implying they are useful. Such models are moderately easy to derive, but have limited applications. The steady-state thermal impedance is critical to calculate maximum junction temperature for a given current and is dependent on the PC board, which is not covered by the spice models accurately. With careful design, a figure close to the steady state junction-to-ambient thermal impedance shown on the datasheet can be attained. With a reasonable area of copper around the

drain leads, and a ground plane, the thermal impedance should be 1.0 to 1.2 times the datasheet value and such rules of thumb are usually sufficiently accurate. The effect of transients (defined as anything less than ~100 seconds in this context) can be taken from the transient thermal impedance curve for transients less than ten seconds as the PC board has minimal effect below ten seconds. Due to the high surge capability of surface mount MOSFETs, high accuracy is seldom required for such pulses. Transients in the ten second to one hundred second range can also be estimated from the transient thermal impedance curve, but this represents an estimate as it is dependent on the thermal characteristics of the PC board. Spice (or other software) thermal modeling is useful for applications such as automotive modules where a substrate is used rather than a PC board. However such thermal modeling (of the heat sink) is the responsibility of the module designer, rather than the MOSFET manufacturer.

The Safe Operating Area (SOA) curves shown on the data sheet are typically simply calculated from the thermal impedance, and absolute maximum ratings for voltage and current. The right hand boundary is the absolute maximum voltage, 30 V for this device. The top boundary is the absolute maximum pulse current which cannot be exceeded for a pulse of any duration. There is also a soft boundary on the upper left where it is not possible to force higher currents for a given voltage due to the on-resistance.

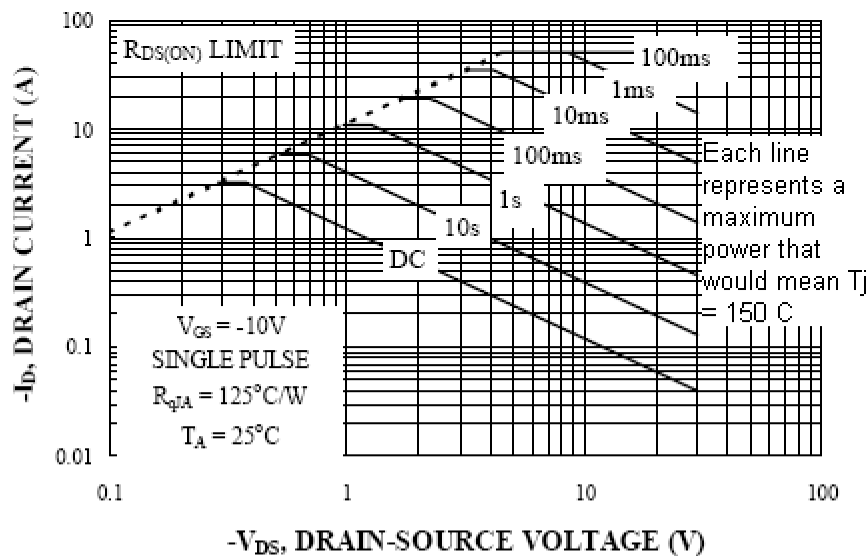


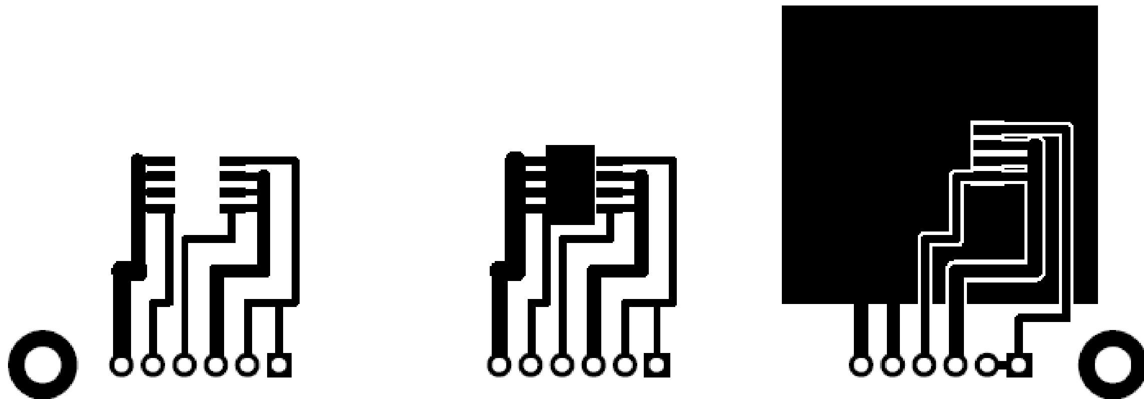
Figure 8. MOSFET SOA curve. Since thee is no second breakdown in Power MOSFETs, the SOA curve can usually be ignored and the maximum single pulse power and transient thermal impedance curves used to ensure that maximum junction temperature is not exceeded.

Surface mount MOSFET thermal ratings given on data sheets are very accurate and useful compared with older packages such as the TO-220. A MOSFET manufacturer would not provide estimates of the performance of a TO-220 and a “typical” (unknown) heat sink, yet that is exactly what manufacturers of surface mount MOSFETs provide. Assuming a reasonable area of copper is used in conjunction with a ground plane, the data sheet steady-state thermal impedance can be used to safely predict operation within the maximum ratings. The packages’ superior pulse power capabilities assist in providing protection against pulses higher than the steady-state power dissipation values, and therefore the steady-state thermal limits are usually the most critical. Packages such as the Analog Power SC70-8J and designs such as the half-bridge AM4520H can be used to achieve lower junction and case temperatures for a given current, or higher currents for a given junction/case temperature. In applications where direct connection to a large area of copper is possible, the Analog Power lead-less SO-8 (SO-8PP) exhibits lower thermal impedance than an SO-8 and will show higher electrical efficiency as a result.

Appendix 1. Steady-State Thermal Impedance Testing For SO-8 Package

An AM4842N N-Channel MOSFET was tested on six different PC board layouts to determine realistic steady-state values for thermal impedance on real-life PC boards. The layouts ranged from minimal traces, and no ground plane, to a solid 1 inch by 1 inch power plane and a solid ground plane on the other side of a two-sided board. Only steady-state thermal impedance values were not measured as the variation due to layouts diminishes as pulse widths are reduced to having very little effect in the one second range.

The three layouts are shown below. They were repeated with a ground plane on the other side of a 2-sided PC board, creating six different layouts. The traces close to the drain pads are 0.040 inch for the minimal layout and 0.060 inch for the heavy/spreader layout which also has solid copper under the device, which will assist in conducting heat to the ground plane.



Scale: approximately 1.5:1

Figure 1. PC Board Layouts. From left to right: Minimal, Heavy/Spreader and Plane. Note Kelvin connections shown but not necessary. Pin 1 is bottom right.

The layouts were tested individually using the MOSFET diode to both heat the device and to measure the temperature increase. The device was mounted on the PC board. A sense-current of 2 mA was applied using a 9V battery and series resistor to ensure no ground bounce or parasitic inductance affected the sense-current. The forward drop of the diode was measured using both a DVM and oscilloscope, the DVM being used as a check only. A known higher current of several amps was then forced through the diode with the “sense” current still flowing.

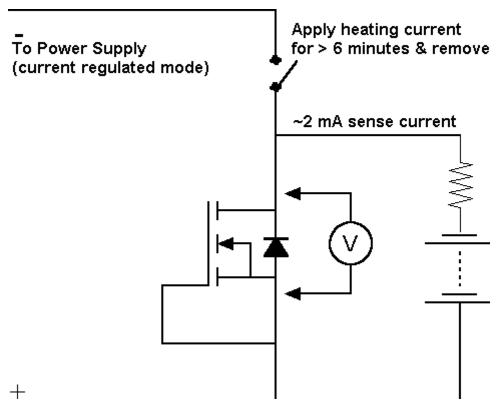


Figure 2. Test Schematic

After approximately six minutes (to ensure steady-state), the total heating current and forward voltage were recorded. The higher current was removed instantaneously while the forward voltage was monitored on the oscilloscope. The forward voltage dropped as the diode current dropped to the sense value. The oscilloscope was set to trigger off this downward step and store the transient. The forward voltage immediately after the higher current was removed was read off the stored oscilloscope display. In this manner, the forward voltage before heating and immediately after heating was recorded, and allowed the change in junction temperature to be recorded using the known variation in forward voltage with temperature. The final heating power was also known (forward current x forward voltage) and since the device had reached steady-state that value can be used for thermal impedance calculations. The readings were repeated several times for each layout and the results averaged. A sample of the actual readings and calculation sis shown below:

board	VSD1	VSD2	I heat	V heat	delta VSD	delta Tj	Power	RTth	W max
plane+plane	0.484	0.285	2.69	0.547	0.199	88.4	1.47143	60.10782	2.079596
plane+no plane	0.471	0.273	2.50	0.542	0.198	88	1.355	64.94465	1.924716

Table 1. Sample of results and calculations.

Delta T_j was calculated using the measured variation in temperature of the MOSFET's diode with temperature of 2.25 mV/°C:

$$\text{delta } T_j = \text{delta } V_{SD}/2.25$$

Rth was calculated using the formula

Rth = delta Tj (° C) / Power (W)

Calculating the values for thermal impedance for each of the layouts gave the following results:

Layout	Steady State Rth	Max Power
	°C/W	W
Device on plane + bottom plane	60	2.07
Device on plane, no bottom plane	64	1.96
Medium layout + bottom plane	70	1.79
Medium layout + no plane	98	1.27
Minimal layout + bottom plane	81	1.54
Minimal layout + no plane	108	1.15

Table 2. Thermal results of layout testing

Several observations are apparent:

1) If a solid ground plane is used on the other side of the board, thermal impedance is improved, especially for a minimal layout.
2) The ground plane has the most effect on the minimal layout, and has only a small improvement for the device mounted on a power plane
3) Even the minimal layout, when used with a ground plane, has a reasonable thermal impedance (81 ºC/W), nearly meeting the data sheet number which applies to a device on a solid 1 inch by 1 inch solid copper plane.
4) The data sheet steady state rating of 80 °C/W (mounted on 1 inch x 1 inch copper) is met with 25% margin.